

SYSTEM FOR HEAD AND TAIL CACHING

ABSTRACT OF THE INVENTION

A head and tail caching system. The system includes a tail FIFO memory having
5 a tail input to receive incoming data. A memory is included that is operable to store data
that is output from the tail FIFO and output the stored data at a memory output. A
multiplexer is included having first and second multiplexer inputs coupled to the tail
FIFO and the memory, respectively. The multiplexer has a control input to select one of
the multiplexer inputs to couple to a multiplexer output. A head FIFO memory receives
10 data from the multiplexer output, and outputs the data on an output data path. A
controller is operable to transfer one or more blocks data having a selected block size
from the tail FIFO to the memory and from the memory to the head FIFO, to achieve a
selected efficiency level.

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